

What is claimed is:

- 1 1. A multi-layer integrated semiconductor structure, comprising:
2 a first semiconductor structure having a plurality of semiconductor elements
3 associated with a first semiconductor signaling technology;
4 a second semiconductor structure having a plurality of semiconductor elements
5 associated with a second semiconductor signaling technology; and
6 an interface disposed to couple a first surface of the first semiconductor structure
7 to a first surface of the second semiconductor structure, wherein the interface includes at
8 least a first portion adapted to provide a communication interface between the first
9 semiconductor structure and the second semiconductor structure and at least a second
10 portion adapted to reduce electrical interference between the first semiconductor structure
11 and the second semiconductor structure.
- 1 2. The multi-layer integrated semiconductor structure of claim 1, wherein the first
2 portion of the interface includes an electrically conductive adhesive material.
- 1 3. The multi-layer integrated semiconductor structure of claim 1, wherein the first
2 portion of the interface includes an electrically conductive material.
- 1 4. The multi-layer integrated semiconductor structure of claim 1, wherein the second
2 portion of the interface includes an electrically conductive adhesive material.
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- 1 5. The multi-layer integrated semiconductor structure of claim 4, wherein the
2 electrically conductive adhesive material is grounded.
- 1 6. The multi-layer integrated semiconductor structure of claim 5, wherein the
2 electrically conductive adhesive material includes at least one of copper, gold, aluminum
3 or a metal alloy.

- 1 7. The multi-layer integrated semiconductor structure of claim 1, wherein the second
2 portion of the interface includes a dielectric adhesive material.
- 1 8. The multi-layer integrated semiconductor structure of claim 7, wherein the
2 dielectric adhesive material includes an organic material.
- 1 9. The multi-layer integrated semiconductor structure of claim 7, wherein the
2 dielectric adhesive material includes an inorganic material.
- 1 10. The multi-layer integrated semiconductor structure of claim 1, wherein the first
2 semiconductor signaling technology includes digital signaling related technology.
- 1 11. The multi-layer integrated semiconductor structure of claim 1, wherein the second
2 semiconductor signaling technology includes analog signaling related technology.
- 1 12. The multi-layer integrated semiconductor structure of claim 1, wherein the
2 interface is adapted to adhesively couple the first surface of the first semiconductor
3 structure to the first surface of the second semiconductor structure.
- 1 13. The multi-layer integrated semiconductor structure of claim 12, wherein the first
2 surface of the first semiconductor structure corresponds to a top surface of the first
3 semiconductor structure.
- 1 14. The multi-layer integrated semiconductor structure of claim 13, wherein the first
2 surface of the second semiconductor structure corresponds to a bottom surface of the
3 second semiconductor structure.
- 1 15. The multi-layer integrated semiconductor structure of claim 13, wherein the first
2 surface of the second semiconductor structure corresponds to a top surface of the
3 second semiconductor structure.

1 16. The multi-layer integrated semiconductor structure of claim 12, wherein the first
2 surface of the first semiconductor structure corresponds to a bottom surface of the first
3 semiconductor structure.

1 17. The multi-layer integrated semiconductor structure of claim 16, wherein the first
2 surface of the second semiconductor structure corresponds a top surface of the second
3 semiconductor structure.

1 18. The multi-layer integrated semiconductor structure of claim 16, wherein the first
2 surface of the second semiconductor structure corresponds to a bottom surface of the
3 second semiconductor structure.

1 19. The multi-layer integrated semiconductor structure of claim 1, further including
2 an adhesive disposed at least between the second portion of the interface and the first
3 surface of the second semiconductor structure.